REMARKS

Claims 1-26 are pending in the application. Claim 19 is allowed. Claims 1-18 and 20-26 have been rejected. Claims 9-11, 13-16, 18, 20, 22, 25 and 26 have been amended, as indicated above, to correct minor informalities.

1. Claim 14 was rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 14 has been amended accordingly.
2. Claims 1-18 and 20-26 were rejected under 35 USC 103(a) as being unpatentable over US Patent No. 6,021,513 (hereinafter "Beebe") in view of US Patent No. 6,829,751 (hereinafter "Shen").

Beebe relates to "a comprehensive test strategy for enabling testing of the configuration subsystems and programmable resources of an FPGA." (Beebe Col. 2:32-35). For example, the testing of Beebe provides a "first test method (B/S or Card test) . . . for testing an FPGA," (Beebe Col. 2:40-43), a "second test method (configuration or LSSD test), the FPGA is provided with a configuration scan chain for testing configuration logic of the FPGA," (Beebe Col. 2:50-52), and a "third test method (array test), [where] the FPGA is provided with repeater scan chains configured within select programmable interconnects of the FPGA," (Beebe Col. 2:61-63). Beebe recites [l]evel-sensitive scan design (LSSD) test techniques [that] are . . . known and involve segmenting a logic circuit into combinational and synchronous logic circuitry." (Beebe col. 3:29-33). In view of the LSSD testing, Beebe seeks "to provide a test strategy which provides adequate testing of the heterogeneous combinational and synchronous resources of an FPGA, enables ready segmentation thereof and overcomes the weakness of using a pure LSSD approach." (Beebe col. 3:29-33).

Shen relates to "a system for designing an integrated circuit (IC) . The system generally comprising a circuit and a programmable portion used for diagnostics and finding bugs. The circuit generally comprises (i) a functional portion and (ii) a logic portion that may be connected to the functional portion to a diagnostic method and/or architecture using an FPGA core in a system on a chip (SOC) design." (Shen Col.

1:55-60). The diagnostic architecture of Shen uses the core "to enable logic to be programmed after the silicon has been produced. The FPGA core can be used to implement on-chip diagnostics to enable debugging functions, such as bus monitoring, probing, single step running, triggering, capturing, etc." (Shen Col. 2:39-42). In other words, the FPGA core of Shen is an extension of a debugging workstation 104. (*See* Shen, Figure 2).

The Office Action stated that "[i]t would have been obvious to one of ordinary skill in the Data Processing art . . . to combine the teachings of Beebe with . . . Shen . . . for testing the fixed logic embedded device in an SOC as taught by Shen." (OA at p. 4).

One problem addressed by the present invention, however, is the testing of ASICs and other complex fixed logic circuits that are at least partially embedded within the FPGA. (*see, e.g.,* Specification ¶¶ 0019, 0025). While the techniques of the present invention may be used to test a simple logic element, one particular embodiment includes an apparatus and corresponding method for testing a more complex fixed logic device. Applicant respectfully submits that the hypothetical combination of the modified-LSSD technique of Beebe and the diagnostic architecture of Shen does not achieve Applicant's claimed invention, *inter alia*, to facilitate a scan chain internally to test an embedded fixed logic device. (*see, e.g.,* Specification ¶ 0060).

For example, the method of Applicant's Independent Claim 1 recites, *inter alia*, a "method for testing circuitry in an FPGA comprising: configuring the FPGA for test including the FPGA forming an FPGA scan chain for simulating an external connection to a fixed logic embedded device; receiving and conducting at least one device scan chain to the embedded device; wherein the at least one device scan chain is for testing the fixed logic embedded device . . . ."

Applicant's Independent Claim 9 recites a "method for testing an FPGA, comprising: configuring internal logic within the FPGA to test an embedded fixed logic device within the FPGA; transmitting a test signal to a multiplexer formed within a gasket; and transmitting the test signal from the multiplexer to the embedded fixed logic device."

Applicant's Independent Claim 14 recites a "method for testing an FPGA, comprising: configuring the FPGA for test and forming a scan chain internal to the FPGA to test a fixed logic embedded device within the FPGA; configuring a multiplexer to receive and forward an output test signal; transmitting the output test signal from the fixed logic embedded device to a multiplexer formed within a gasket; and transmitting the output test signal from the multiplexer to an FPGA fabric portion."

Applicant's Independent Claim 20 recites, *inter alia*, an "FPGA, comprising: an FPGA fabric portion; a gasket formed at least partially within the FPGA fabric portion, the gasket forming interfacing logic between an embedded core device and the fabric portion; and at least one multiplexer coupled serially between the FPGA fabric portion and the embedded core device."

Accordingly, there is no suggestion or motivation in the modified-LSSD technique of Beebe and the diagnostic architecture of Shen to combine these references to achieve Applicant's claimed invention. Further, all the elements of Applicant's claimed invention are not present in the hypothetical combination of Beebe and Shen. These references, neither separately nor in combination, do not address a problem solved by the embodiments of the present invention, namely, the testing of complex fixed logic circuitry embedded within an FPGA that is otherwise configurable. *See* MPEP § 2142, p. 2100-128 (Rev. 2, May 2004).

Applicant respectfully submits that a prima facie showing has not been made with respect to the method of Independent Claim 1 and Claims 2-8 that depend directly or indirectly therefrom, the method of Independent Claim 9 and Claims 10-13 that depend directly or indirectly therefrom, the method of Independent Claim 14 and Claims 15-18 that depend directly or indirectly therefrom, and the FPGA of Independent Claim 20 and Claims 21-26 that depend directly or indirectly therefrom.

3. Allowable Subject Matter

Applicant notes with appreciation the allowance of Claim 19.

4. Conclusion

As a result of the foregoing, the Applicant respectfully submits that Claims 1-18 and 20-26 are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on July 27, 2005.

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